NMTSim: Transaction-Command based Simulator for New Memory Technology Devices

Peng Gu[1], Benjamin S. Lim[2]

Wenqin Huangfu[1], Krishna T. Malladi[2], Andrew Chang[2], Yuan Xie[1]

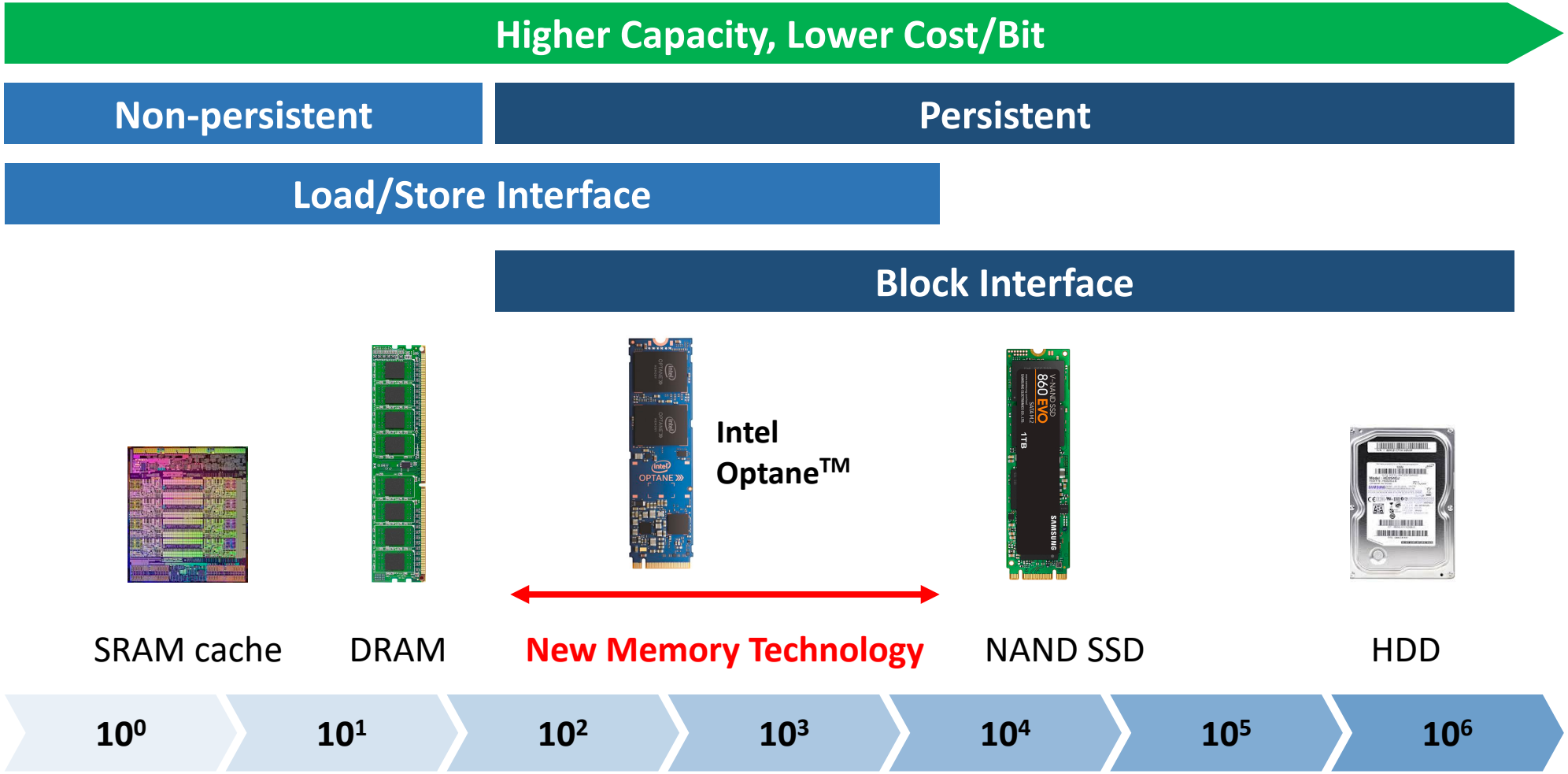
[1]University of California, Santa Barbara

[2]Samsung Semiconductor

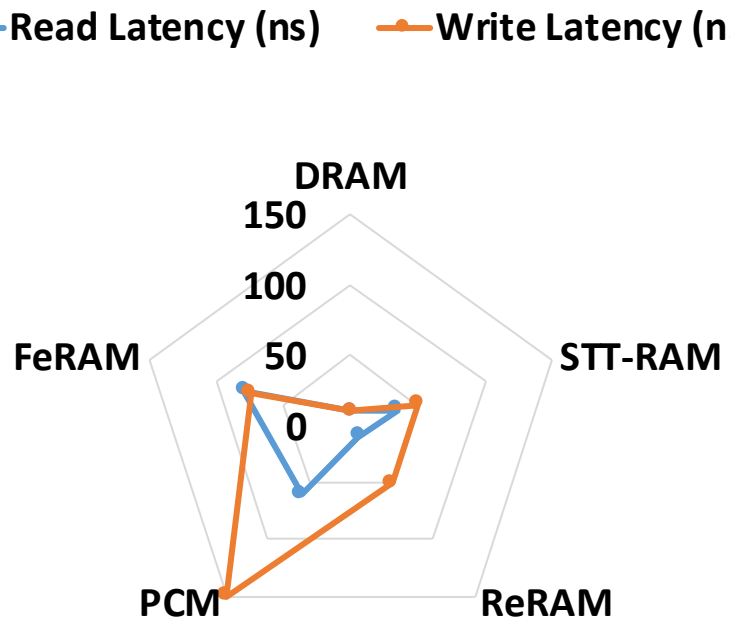
UC Santa Barbara
Scalable Energy-efficient Architecture Lab

SAMSUNG

New Non-volatile Memory Technologies



New Non-volatile Memory Technologies



	Read Latency	Write latency
HDD	3-5 ms	3-5 ms
NAND FLASH	15-35 us	200-50 us

Key benefits:

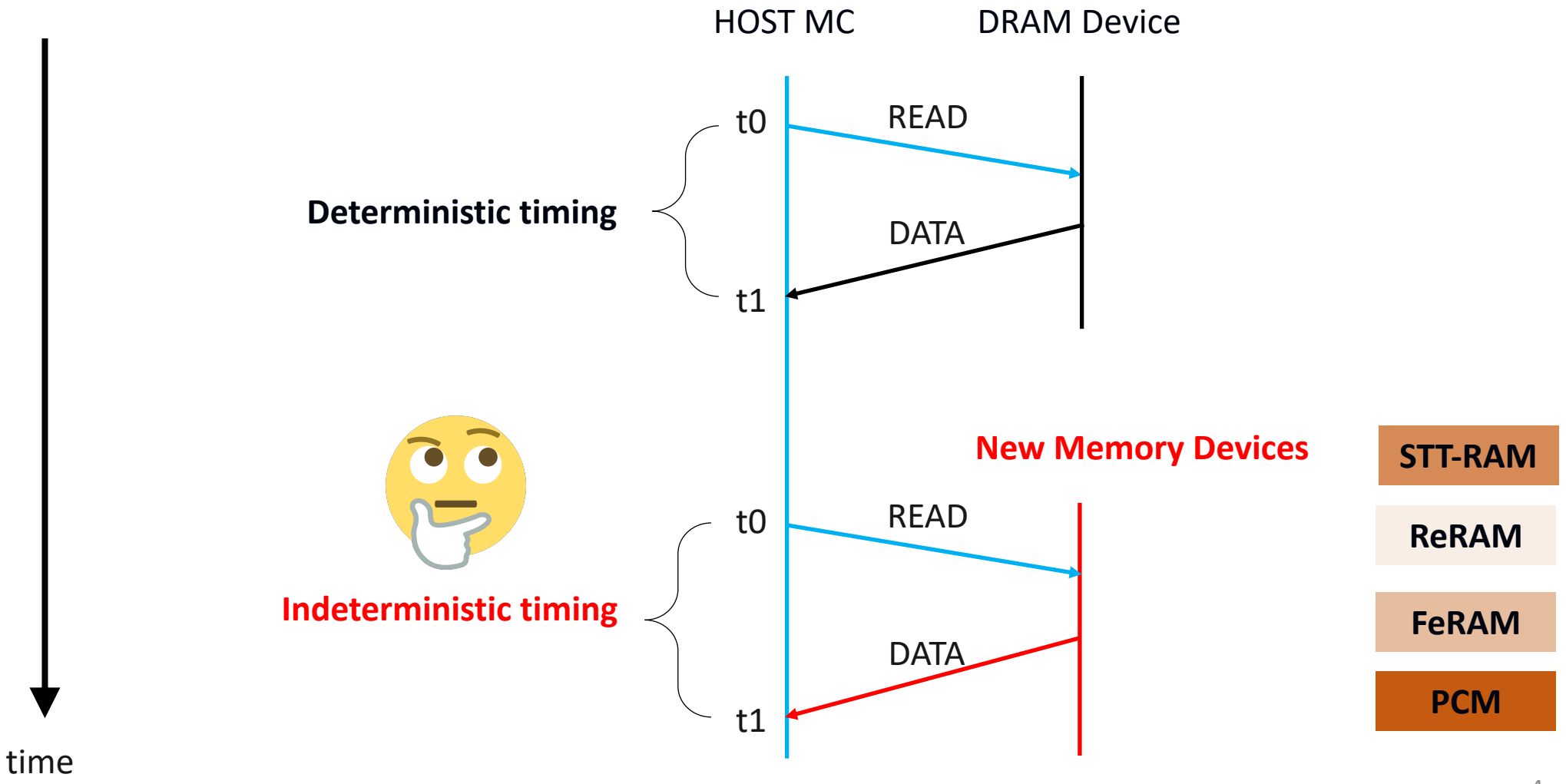
- Significant performance improvement
- Potential to augment main memory

Challenges:

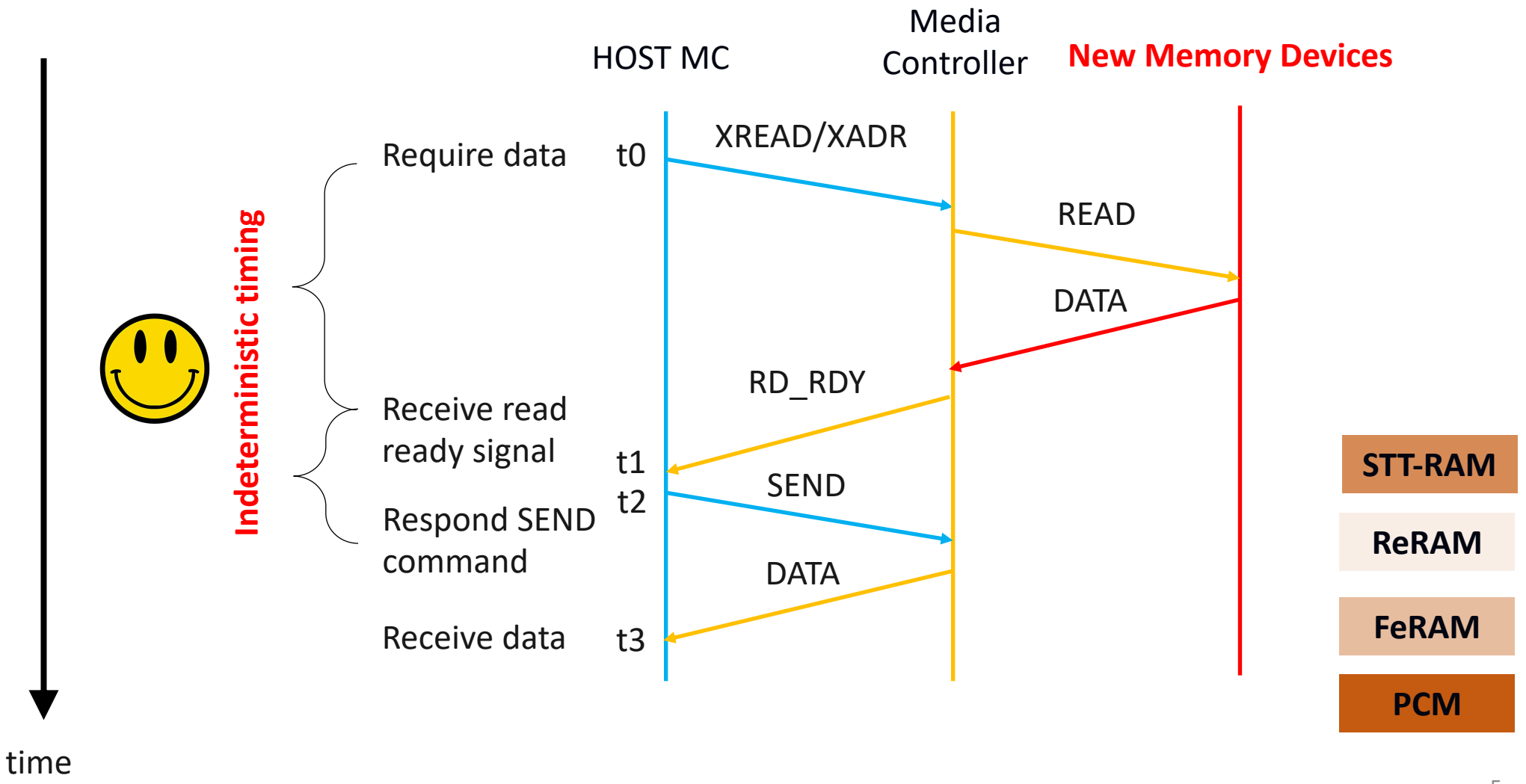
- Traditional DDR interface uses deterministic timing. How to tolerate different media access latency?

"Emerging NVM: A Survey on Architectural Integration and Research Challenges"

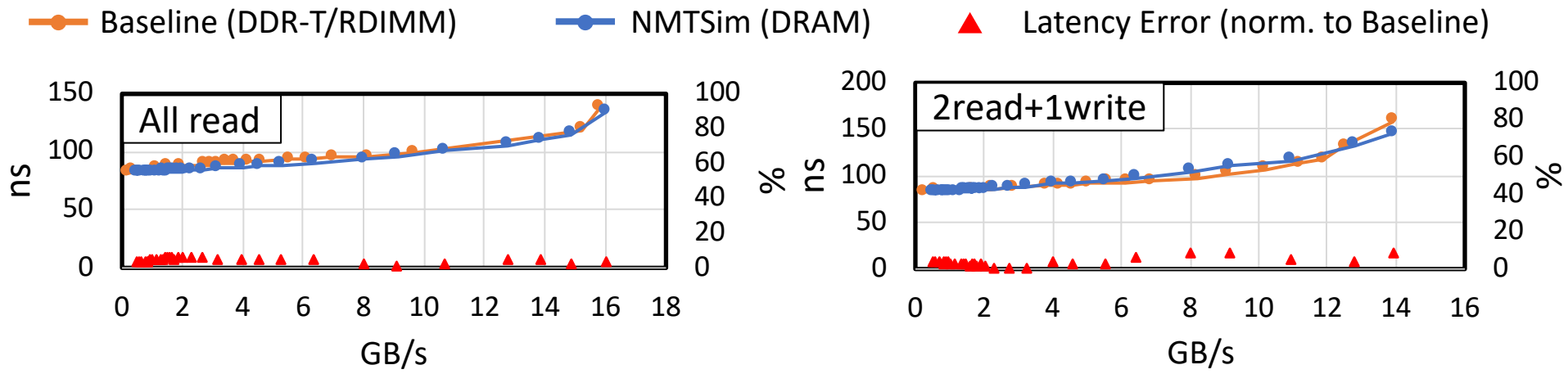
Traditional DRAM simulator



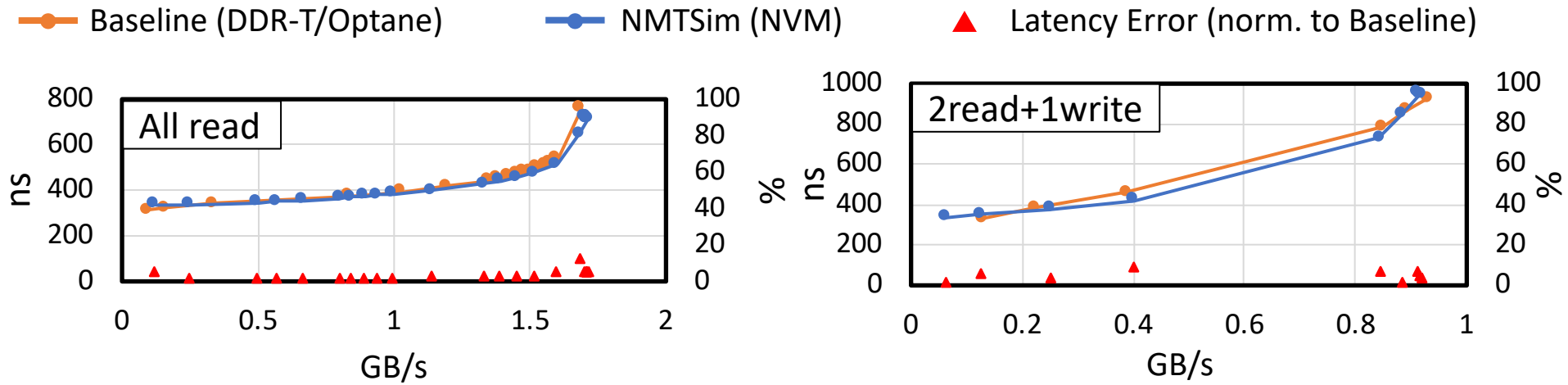
NMTSim: Transaction Command Simulator



NMTSim validation

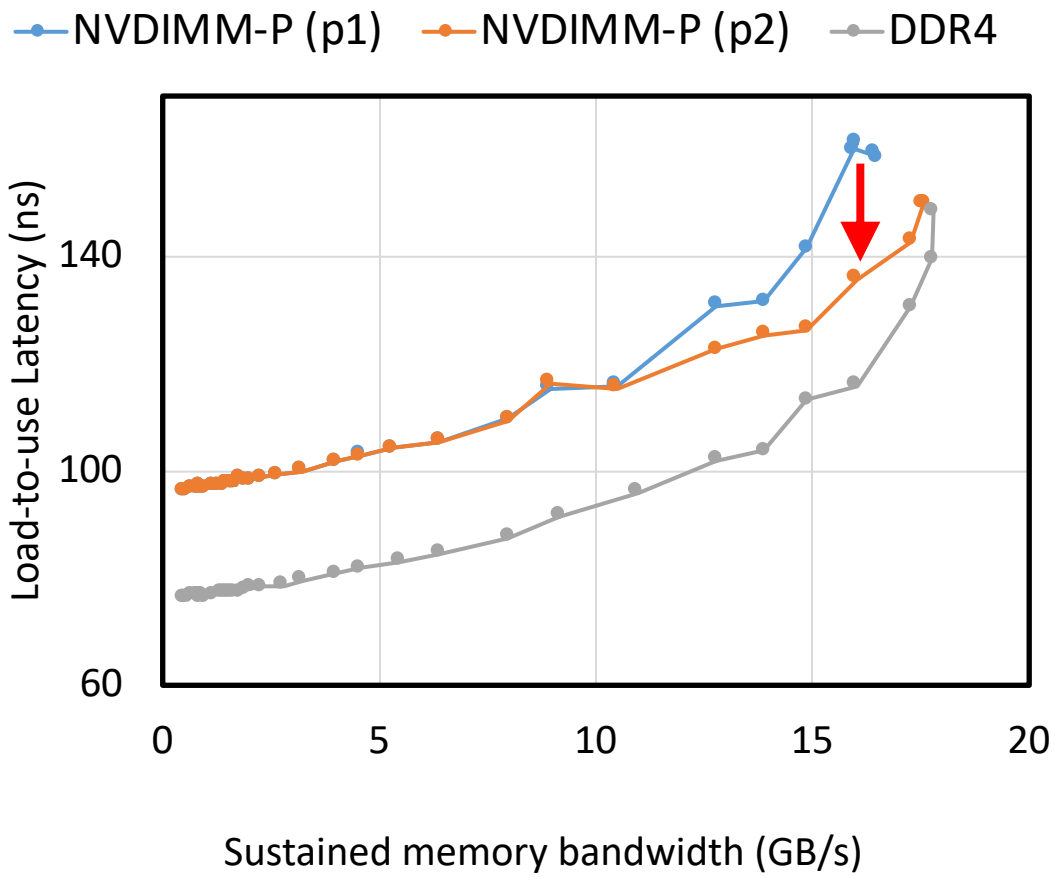


2.8% latency error for *DRAM* device



3.4% latency error for *NVM* device

NMTSim optimizations



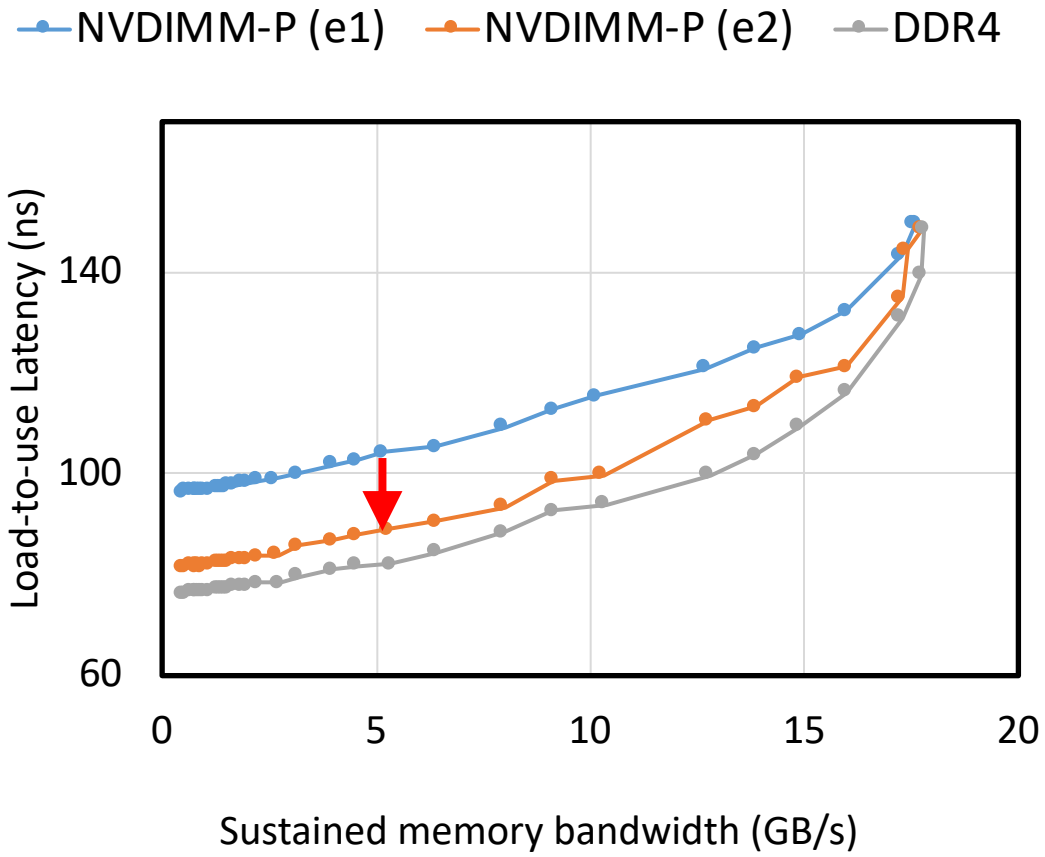
Command Issue Priority:

- p1: XREAD > SEND
- p2: SEND > XREAD

Takeaway:

- Reduce response queuing latency is important in latency reduction at high memory rates

NMTSim optimizations



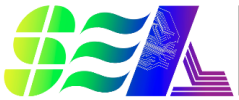
- e1: No early notification
- e2: Early notification enabled

Takeaway:

- Enabling early notification helps reduce latency significantly

NMTSim: Transaction-Command based Simulator for New Memory Technology Devices

Thank you!



UC Santa Barbara
Scalable Energy-efficient
Architecture Lab